UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/281,042	03/30/1999	SEIKI AGURO	TIJ-26495	6678

23494 7590 07/12/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
JONES, HUGH M	

ART UNIT	PAPER NUMBER
2128	35

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/281,042	Applicant(s) AGURO, SEIKI	
	Examiner Hugh Jones	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 4-21 of U. S. Application 08/281,042 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 8, 10, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al. (U.S. Patent 4,700,296) in view of Hyatt (U. S. Patent 4,942,516).

As regards Claim 8 the Palmer, Jr. et al. reference discloses an integrated circuit computer system (Figure 2, Item 6i) having a processor interconnected with memory (Figure 1, Item 6d and Col. 5 Lines 32-65) and peripheral circuits on said integrated circuit (Figure 1 Items 6f and 6c and 6a) coupled to a security system (Figures 1-6 and Col. 1 Lines 30-61) comprising:

a plurality of input ports for said processor, (Figure 1 Items 6b, 6c, 6d, 6e note the direction of the arrows to the Process Control Program and Col. 2 Lines 50-68 and Col. 3 Lines 1-4).

a program stored in said memory to operate said processor (Figure 1, Process Control Program and Item 6d Code Table (ROM)), to receive a plurality of commands to said plurality of input ports to produce a password (Figure 1 Items 6c, Item 4 and Figure 2 Item 6c and Figure 4 and Figure 5 and Col. 1 Lines 37-56 and Col. 5 Lines 32-65) which is compared with a predetermined password (Figure 2 Item labeled LOOK-UP TABLE and Col. 7 Lines 33-38).

As regards Claims 10, 15, the Palmer, Jr. et al. reference inherently discloses a specified time sequence.

As regards Claim 14, Palmer Jr. et al. reference teaches; A security system for an integrated circuit computer system (All of Figures 1, 2 and 3 and Col. 2 Lines 50-54) comprising: applying a plurality of commands to a plurality of ports for a processor of said system (Figure 1 Items 6a, the block labeled PROCESS CONTROL PROGRAM, Item 4, Item 6f); a program stored in a memory coupled to said processor for operating said processor to process said plurality of commands to produce a password; (Figure 2 Item 6i and Item 6c and Col. 1 Lines 37-56); comparing said produced password with a predetermined password (Figure 1 Item 6 PARAMETER STORAGE REGISTERS, and Figure 2, Item 6i PARAMETER STORAGE and Col. 8 Lines 12-32).

5. The applied references do not expressly disclose the use of a single chip.

6. Hyatt discloses a single chip integrated circuit.

7. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the references to include the use of a single chip for the reasons provided by Hyatt at col. 1, lines 48-58 and col. 5, line 54 to col. 6, line 34.

8. Claims 8, 10, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Angelo in view of Hyatt.

Angelo discloses a method for enabling power to all or portions of a computer system based upon the results of a two-piece user verification process that is completed as part of a secure power-up procedure. ***At some point during the secure power-up procedure, the computer user provides an external token or smart card that is coupled to the computer through specialized hardware.*** The token or smart card is used to store an encryption algorithm furnished with an encryption key that is unique or of limited production. ***The computer user is then required to enter a plain text user password. Once entered, the user password is encrypted using the encryption algorithm contained in the external token to create a system password. The system password is compared to a value stored in secure memory***. If the two values match, the power-on sequence is completed and power to the computer system and/or secured computer resources is enabled. If the two values do not match, power to the entire computer system and/or secured computer resources is disabled. The two-piece nature of the authorization process requires the presence of both the user password and the external token in order to generate the system password. ***Angelo also discloses (col. 9) that when the user is prompted to enter a plain text power-on password, as an alternative to a memorized value, the plain text password***

could be generated with the aid of biometrics. For example, a scanned fingerprint could be converted into a plain text password value. See col. 1-2 for general background; col. 3, lines 16-36; fig. 2 and corresponding text; col. 7-9.

9. The applied references do not expressly disclose the use of a single chip.

10. Hyatt discloses a single chip integrated circuit.

11. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the references to include the use of a single chip for the reasons provided by Hyatt at col. 1, lines 48-58 and col. 5, line 54 to col. 6, line 34.

12. Claims 4, 5, 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al. U.S. Patent 4,700,296 in view of Hyatt and in further view of Raghavavhari U.S. Patent 5,774,545.

As regards Claim 4 the Palmer, Jr. et al. reference discloses an integrated circuit computer system (Figure 2, Item 6i) having a processor interconnected with memory (Figure 1, Item 6d and Col. 5 Lines 32-65) and peripheral circuits on said integrated circuit (Figure 1 Items 6f and 6c and 6a). A security means (Figures 1-6 and Col. 1 Lines 30-61) comprising: a plurality of input ports for said processor (Figure 1 Items 6b, 6c, 6d, 6e note the direction of the arrows to the Process Control Program and Col. 2 Lines 50-68 and Col. 3 Lines 1-4); a program stored in said memory to operate said processor (Figure 1, Process Control Program and Item 6d Code Table (ROM)), to receive a plurality of commands to said plurality of input ports to process said commands to produce a password (Figure 1 Items 6c, Item 4 and Figure 2 Item 6c and Figure 4 and Figure 5 and Col. 1 Lines 37-56 and Col. 5 Lines 32-65) which is

compared with a predetermined password (Figure 2 Item labeled LOOK-UP TABLE and Col. 7 Lines 33-38), and a switching circuit is responsive to said comparison (Col. 4 Lines 36-50).

13. The applied references do not expressly disclose the use of a single chip.

14. Hyatt discloses a single chip integrated circuit.

15. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the references to include the use of a single chip for the reasons provided by Hyatt at col. 1, lines 48-58 and col. 5, line 54 to col. 6, line 34.

16. The Palmer, Jr. et al. reference does not expressly disclose, a scan-path interface circuit for reading out the predetermined memory or register in said system.

17. The Raghavachari reference discloses that many integrated circuits are accessed via scan ports and specifically discloses a scan-path interface circuit (Figure 1 Item 15 and Col. 13 Lines 10-13) as part of a security system requiring password authentication through comparison of an input password from an external device with a pre-stored password (Figures 1-10 and Col. 13 Lines 4-67 and Col. 14 Lines 1-67 and Col. 15 Lines 1-29 and Col. 16 Lines 1-29).

18. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have combined the Palmer, Jr. et al. reference with the Raghavachari reference because, (motivation to combine) by protecting the scan-path interface with a password the integrated circuit is rendered useless to those who cannot meet the random security challenge and therefore reduces the value of the integrated circuit to potential thieves, (Raghavachari, Col. 1 Lines 45-61).

19. As regards Claim 9 the Palmer, Jr. et al. reference does not expressly disclose a switching circuit coupled to said scan-path interface.

20. The Raghavachari reference discloses that many integrated circuits are accessed via scan ports and specifically discloses a switching circuit coupled to said scan-path interface (Figure 1 Items 15 and 13, Figure 5 Items 56, 55, 51, Figure 8 Items 81, 82, 83 and Col. 2 Lines 60-67, Col. 3 Lines 1-40), and responsive to said comparison for switching said scan-path interface circuit (Figure 5 and Col. 7 Lines 30-41), between a first mode in which it is enabled (Figure 9, note the control flow diamond decision symbol that states "PASSWORDS MATCH?" after this symbol, follow the arrow for the, YES result, to the computational steps rectangle symbol wherein, the item labeled "1. UNLOCK THE DEVICE") and a second mode in which it is disabled (Figure 9, note the control flow diamond decision symbol that states "PASSWORDS MATCH?" after this symbol, follow the arrow to the, NO result to the computational steps rectangle symbol wherein, the item labeled "1.INCREMENT FAILURE COUNT REGISTER, follow the arrows in the flow chart to the control decision symbol that states "SECURITY PASSWORD RECEIVED" and note that a, NO result, creates a loop back into that control decision symbol and NEVER sets the needed bits in the SECURITY STATUS REGISTER required to enable the scan-path port to operate).

21. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have combined the Palmer, Jr. et al. reference with the Raghavachari reference because, (motivation to combine) by protecting the scan-path interface with a password the integrated circuit is rendered useless to those who cannot meet the

random security challenge and therefore reduces the value of the integrated circuit to potential thieves, (Raghavachari, Col. 1 Lines 45-61).

22. As regards Claims 5, the Palmer, Jr. et al. reference inherently discloses a specified time sequence.

23. The Raghavachari reference also discloses receiving a plurality of commands which are applied to said plurality of ports in a specific time sequence (Figures 9, 10 and Col. 9 Lines 49-66, Col. 10 Lines 1-67, Col. 11 Lines 1-67, Col. 12 Lines 1-60).

24. Claims 6, 7, 11, 12, 13, 16, 17, 19, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al. U.S. Patent 4,700,296 in view of Hyatt and Raghavavhari U.S. Patent 5,774,545 and in further view of Jacobson et al. U.S. Patent 5,784,577.

25. As regards Claims 6, 7, 11, 12, 13, 16 and 17 the Palmer et al. reference does not expressly disclose; a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers.

26. The Jacobson et al. reference discloses; a pair of registers (Figure 3, Items 301 and 302), one of said registers receiving said produced password (Figure 3 Item 302) and the other of said registers containing said predetermined password (Figure 3 Item 301) a comparator for comparing the contents of said registers (Figure 3 Item 303) for controlling a Data Protect Circuitry (Figure 3 Item 306).

27. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have combined the Palmer, Jr. et al. reference with the Jacobson et al.

reference because, (motivation to combine) a need arises for an accurate, overridable method of tracking versions of the PLDs, as well as preventing unauthorized users from programming the PLDs, (Jacobson et al. Col. 2 Lines 10-13).

28. As regards Claims 19, 20 and 21, the Palmer, Jr. et al. reference does not expressly disclose; a scan-path interface circuit for comparison with a predetermined memory or register, and a switching circuit that is responsive to said comparison to switch operation of said scan-path interface between enabled and disabled modes. (It is noted by the examiner that the Palmer, Jr. et al. reference does disclose a switching circuit and a comparison of a predetermined memory or register, responsive to said comparison of an externally provided password with a predetermined password, the ONLY limitation not disclosed in the Palmer, Jr. et al. reference is a scan-path interface).

29. The Jacobson et al. reference discloses a scan-path interface circuit (Col. 1 Lines 42-55, Col. 4 Lines 39-42) for reading out contents of a predetermined memory or register in said system (Figure 3, Item 300 and Col. 2 Lines 15-45) and a switching circuit responsive to said comparison to switch operation of said scan-path interface between enabled and disabled modes, (all of Figure 3 and Figure 2 and Col. 3 Lines 14-67, Col. 4 Lines 1-49).

30. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the Palmer, Jr. et al. reference with the Jacobson et al. reference because, (motivation to combine) ...a need arises for an accurate, overridable

method of tracking versions of the PLDs, as well as preventing unauthorized users from programming the PLDs (Jacobson et al. Col. 2 Lines 11-13).

31. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al. U.S. Patent 4,700,296 view of Hyatt and in further view of Jacobson et al. U.S. Patent 5,784,577.

32. The Palmer, Jr. et al. reference does not expressly disclose; a scan-path interface circuit for comparison with a predetermined memory or register, and a switching circuit that is responsive to said comparison to switch operation of said scan-path interface between enabled and disabled modes. (It is noted by the examiner that the Palmer, Jr. et al. reference does disclose a switching circuit and a comparison of a predetermined memory or register, responsive to said comparison of an externally provided password with a predetermined password, the ONLY limitation not disclosed in the Palmer, Jr. et al. reference is a scan-path interface).

33. The Jacobson et al. reference discloses a scan-path interface circuit (Col. 1 Lines 42-55, Col. 4 Lines 39-42) for reading out contents of a predetermined memory or register in said system (Figure 3, Item 300 and Col. 2 Lines 15-45) and a switching circuit responsive to said comparison to switch operation of said scan-path interface between enabled and disabled modes, (all of Figure 3 and Figure 2 and Col. 3 Lines 14-67, Col. 4 Lines 1-49).

34. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the Palmer, Jr. et al. reference with the Jacobson et al. reference because, (motivation to combine) ...a need arises for an accurate, overridable

method of tracking versions of the PLDs, as well as preventing unauthorized users from programming the PLDs (Jacobson et al. Col. 2 Lines 11-13).

35. Claims 4-7, 9, 11-13, 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Angelo in view of Hyatt and in further view of Bianco et al..

34. Angelo discloses a method for enabling power to all or portions of a computer system based upon the results of a two-piece user verification process that is completed as part of a secure power-up procedure. ***At some point during the secure power-up procedure, the computer user provides an external token or smart card that is coupled to the computer through specialized hardware.*** The token or smart card is used to store an encryption algorithm furnished with an encryption key that is unique or of limited production. ***The computer user is then required to enter a plain text user password. Once entered, the user password is encrypted using the encryption algorithm contained in the external token to create a system password. The system password is compared to a value stored in secure memory***. If the two values match, the power-on sequence is completed and power to the computer system and/or secured computer resources is enabled. If the two values do not match, power to the entire computer system and/or secured computer resources is disabled. The two-piece nature of the authorization process requires the presence of both the user password and the external token in order to generate the system password. *Angelo also discloses (col. 9) that when the user is prompted to enter a plain text power-on password, as an alternative to a memorized value, the plain text password could be generated with the aid of biometrics. For example, a scanned fingerprint could be*

converted into a plain text password value. See col. 1-2 for general background; col. 3, lines 16-36; fig. 2 and corresponding text; col. 7-9.

35. The applied references do not expressly disclose the use of a single chip.

36. Hyatt discloses a single chip integrated circuit.

37. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the references to include the use of a single chip for the reasons provided by Hyatt at col. 1, lines 48-58 and col. 5, line 54 to col. 6, line 34.

38. Angelo does not expressly disclose; a *scan-path* interface circuit for comparison with a predetermined memory or register, and a switching circuit that is responsive to said comparison to *switch operation of said scan-path* interface between enabled and disabled modes.

39. Bianco et al. disclose a set/scan test capability which is provided for a circuit that includes sensitive subcircuits, but that can be latched out to prevent reverse engineering the sensitive elements. A mechanism to inhibit set/scan test access to at least some of the sensitive subcircuits is selectively actuated by a control circuit to override a normal set/scan test and inhibit set/scan access to the sensitive subcircuits. Various implementations are possible, such as fusible-link PROMs for irreversibly inhibiting set/scan access to the sensitive subcircuits after an initial non-inhibited test period, the use of encryption codes to enable repeated set/scan access to the sensitive subcircuits, and an erasable/reprogrammable mechanism for inhibiting set/scan access to programmed sets of subcircuits. See col. 1 to col. 2, line 26 for need to protect integrated circuits; col. 2, line 29 to col. 3, line 8; fig. 6 and corresponding text.1

40. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the Angelo reference with the Bianco et al. reference (motivation to combine) for the following reasons. Bianco states that integrated circuitry is subject to reverse engineering and should be protected (col. 1-2). Bianco discloses enhancing the testability of ICs that contain sensitive circuitry through the use of the set/scan test technique, while preventing the disclosure of the sensitive circuitry design to unauthorized parties. In so doing the invention allows sensitive subcircuits to be removed from the set/scan test chain. The removal can be permanent, or the sensitive subcircuits can be included in the set/scan chain in response to the application of a control code by an authorized user. The manufacturer is provided with full testability during device fabrication, while access to the sensitive elements can be restricted once the device is delivered; copiers are thereby prevented from exploiting the set/scan capability to obtain design details required for the production of unauthorized copies. The invention is compatible with, and enhances the strength of, other anti-reverse engineering measures such as opaque die coatings or the techniques disclosed in U.S. Pat. No. 4,766,516. Bianco discloses the need for a mechanism to inhibit set/scan test access to at least some of the IC's sensitive subcircuits, and a mechanism for overriding a normal set/scan test by actuating the inhibit mechanism for the sensitive subcircuits while permitting set/scan access to the remaining subcircuits.

Response to Argument – prior art rejections

41. Appellant's arguments with respect to the claims (paper # 34 - amendment) have been considered but are not persuasive.

42. Applicant's argument in paper # 34 is that the issue of "single-chip" was newly raised in the Examiner's answer. The issue was addressed because Applicant's first raised the issue in the Appeal Brief. The Examiner's Answer provided no indication that the "single-chip" feature was novel or non-obvious in the context of the claims. The issue was never previously addressed because the feature was never claimed.

43. It is noted that merely implementing an invention on a single chip, in and of itself, does not render the claimed invention novel or non-obvious over the prior art of record. See MPEP 2144.04 (Making Integral).

44. Appellant's arguments with respect to the claims (paper 31 – Appeal Brief) have been considered but are not persuasive.

45. Appellant's arguments relating to the Palmer 102 rejection are noted, but are not persuasive. Palmer, Jr. et al. reference discloses an integrated circuit computer system (Figure 2, Item 6i) having a processor interconnected with memory (Figure 1, Item 6d and Col. 5 Lines 32-65) and peripheral circuits on said integrated circuit (Figure 1 Items 6f and 6c and 6a). A security means (Figures 1-6 and Col. 1 Lines 30-61) comprising: a plurality of input ports for said processor (Figure 1 Items 6b, 6c, 6d, 6e note the direction of the arrows to the Process Control Program and Col. 2 Lines 50-68 and Col. 3 Lines 1-4); a program stored in said memory to operate said processor (Figure 1, Process Control Program and Item 6d Code Table (ROM)), to receive a plurality of

commands to said plurality of input ports to process said commands to produce a password (Figure 1 Items 6c, Item 4 and Figure 2 Item 6c and Figure 4 and Figure 5 and Col. 1 Lines 37-56 and Col. 5 Lines 32-65) which is compared with a predetermined password (Figure 2 Item labeled LOOK-UP TABLE and Col. 7 Lines 33-38), and a switching circuit is responsive to said comparison (Col. 4 Lines 36-50). Appellants, respectfully, appear to be reading in definitions which are not reflected in the claims. For example, if Appellants feel that port only means " a group of I/O pins...", then that feature should be recited in the claims.

46. Appellants conclude their arguments with abstract hypothetical arguments (see page 8, paper # 31 – Appeal Brief, for example) relating to "reversed situations". The Examiner, respectfully, will not address such hypothetical arguments.

47. Appellant's arguments relating to the Angelo et al. rejection are noted, but are not persuasive. The argument that Angelo does not disclose an integrated circuit computer system is simply not persuasive. Angelo discloses a method for enabling power to all or portions of a computer system based upon the results of a two-piece user verification process that is completed as part of a secure power-up procedure. ***At some point during the secure power-up procedure, the computer user provides an external token or smart card that is coupled to the computer through specialized hardware.*** The token or smart card is used to store an encryption algorithm furnished with an encryption key that is unique or of limited production. ***The computer user is then required to enter a plain text user password. Once entered, the user password is encrypted using the encryption algorithm contained in the external***

token to create a system password. The system password is compared to a value stored in secure memory. If the two values match, the power-on sequence is completed and power to the computer system and/or secured computer resources is enabled. If the two values do not match, power to the entire computer system and/or secured computer resources is disabled. The two-piece nature of the authorization process requires the presence of both the user password and the external token in order to generate the system password. *Angelo also discloses (col. 9) that when the user is prompted to enter a plain text power-on password, as an alternative to a memorized value, the plain text password could be generated with the aid of biometrics. For example, a scanned fingerprint could be converted into a plain text password value.* See col. 1-2 for general background; col. 3, lines 16-36; fig. 2 and corresponding text; col. 7-9.

48. The arguments against the 103 rejections are not persuasive. The arguments against Palmer have been addressed earlier.

49. The Raghavachari reference discloses that many integrated circuits are accessed via scan ports and specifically discloses a scan-path interface circuit (Figure 1 Item 15 and Col. 13 Lines 10-13) as part of a security system requiring password authentication through comparison of an input password from an external device with a pre-stored password (Figures 1-10 and Col. 13 Lines 4-67 and Col. 14 Lines 1-67 and Col. 15 Lines 1-29 and Col. 16 Lines 1-29).

50. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have combined the Palmer, Jr. et al. reference with the Raghavachari

reference because, (motivation to combine) by protecting the scan-path interface with a password the integrated circuit is rendered useless to those who cannot meet the random security challenge and therefore reduces the value of the integrated circuit to potential thieves, (Raghavachari, Col. 1 Lines 45-61).

51. The Raghavachari reference discloses that many integrated circuits are accessed via scan ports and specifically discloses a switching circuit coupled to said scan-path interface (Figure 1 Items 15 and 13, Figure 5 Items 56, 55, 51, Figure 8 Items 81, 82, 83 and Col. 2 Lines 60-67, Col. 3 Lines 1-40), and responsive to said comparison for switching said scan-path interface circuit (Figure 5 and Col. 7 Lines 30-41), between a first mode in which it is enabled (Figure 9, note the control flow diamond decision symbol that states "PASSWORDS MATCH?" after this symbol, follow the arrow for the, YES result, to the computational steps rectangle symbol wherein, the item labeled "1. UNLOCK THE DEVICE") and a second mode in which it is disabled (Figure 9, note the control flow diamond decision symbol that states "PASSWORDS MATCH?" after this symbol, follow the arrow to the, NO result to the computational steps rectangle symbol wherein, the item labeled "1.INCREMENT FAILURE COUNT REGISTER, follow the arrows in the flow chart to the control decision symbol that states "SECURITY PASSWORD RECEIVED" and note that a, NO result, creates a loop back into that control decision symbol and NEVER sets the needed bits in the SECURITY STATUS REGISTER required to enable the scan-path port to operate).

52. Bianco et al. disclose a set/scan test capability which is provided for a circuit that includes sensitive subcircuits, but that can be latched out to prevent reverse

engineering the sensitive elements. A mechanism to inhibit set/scan test access to at least some of the sensitive subcircuits is selectively actuated by a control circuit to override a normal set/scan test and inhibit set/scan access to the sensitive subcircuits. Various implementations are possible, such as fusible-link PROMs for irreversibly inhibiting set/scan access to the sensitive subcircuits after an initial non-inhibited test period, the use of encryption codes to enable repeated set/scan access to the sensitive subcircuits, and an erasable/reprogrammable mechanism for inhibiting set/scan access to programmed sets of subcircuits. See col. 1 to col. 2, line 26 for need to protect integrated circuits; col. 2, line 29 to col. 3, line 8; fig. 6 and corresponding text.1

53. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the Angelo reference with the Bianco et al. reference (motivation to combine) for the following reasons. Bianco states that integrated circuitry is subject to reverse engineering and should be protected (col. 1-2). Bianco discloses enhancing the testability of ICs that contain sensitive circuitry through the use of the set/scan test technique, while preventing the disclosure of the sensitive circuitry design to unauthorized parties. In so doing the invention allows sensitive subcircuits to be removed from the set/scan test chain. The removal can be permanent, or the sensitive subcircuits can be included in the set/scan chain in response to the application of a control code by an authorized user. The manufacturer is provided with full testability during device fabrication, while access to the sensitive elements can be restricted once the device is delivered; copiers are thereby prevented from exploiting the set/scan capability to obtain design details required for the production of unauthorized copies.

The invention is compatible with, and enhances the strength of, other anti-reverse engineering measures such as opaque die coatings or the techniques disclosed in U.S. Pat. No. 4,766,516. Bianco discloses the need for a mechanism to inhibit set/scan test access to at least some of the IC's sensitive subcircuits, and a mechanism for overriding a normal set/scan test by actuating the inhibit mechanism for the sensitive subcircuits while permitting set/scan access to the remaining subcircuits.

54. The argument that the system of Bianco requires more circuitry or is less elegant is, respectfully, irrelevant.

55. The allegations on page 13 of the Appeal Brief, respectfully, do not distinguish the claims over the prior art.

Conclusion

56. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to: Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to 0700 ET, ***or*** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to: Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 308-9051 (for formal communications intended for entry) ***or***

(703) 308-1396 (for informal or draft communications, please label "*PROPOSED*" or "*DRAFT*").

Dr. Hugh Jones

Primary Patent Examiner

July 3, 2004